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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,122	09/21/2000	William C. Moyer	SC11306TH	9170

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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/667,122	MOYER ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-21 and 23-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-9,13,15-17,21 and 23-26* is/are allowed.

6)☒ Claim(s) *10-12 and 18-20* is/are rejected.

7)☒ Claim(s) *27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13, 15-21, and 23-27 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 1/30/2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 10-12 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida, U.S. Patent No. 6,205,536. In addition, Hennessy is cited as extrinsic evidence for providing a showing that prediction signals and predicted addresses are provided with each other in the same cycle.

5. Referring to claim 10, Yoshida has taught a processing system for fetching instructions and data, comprising:

a) an address bus for providing a current address for retrieving a first instruction, the first instruction stored at the current address in an instruction memory (Fig.26, component 11), a previous address for retrieving a second instruction, the second instruction stored at the previous

address in the instruction memory (Fig.26, component 11), and a data address for retrieving data, wherein the data address occurs before the current address and after the previous address, and wherein the current address follows the previous address without any intervening addresses for retrieving instructions. See the abstract and Fig.27 and note that the third address provided is a data address, and it occurs between a previous and current address. Note that no intervening instruction addresses exist between instruction addresses 2 and 3.

b) a data bus for retrieving the first and second instructions and the data. This is an inherent component as data and instructions must be transmitted via some medium.

c) a fetch unit, coupled to the address bus and the data bus, for generating a first sequence signal that when asserted for the current address indicates that the current address is sequential to the previous address and when negated indicates that the current address may not be sequential to the previous address, wherein the asserted or negated first sequence signal is provided with the current address for use by the instruction memory. Note from column 10, lines 30-36, that Yoshida has taught branch prediction for branch instructions, which would be a type of instruction represented in Fig.27. Even though Yoshida is silent as to how the branch prediction (first signal) is performed, it is inherent that when predicting branches, they may be predicted taken or not taken. Clearly, if a branch is predicted not taken, then the current address is sequential to the previous address. That is, the system begins fetching from the address immediately following the address of the branch instruction (the current address is used by the instruction memory). On the other hand, if the branch is predicted taken, then the current address may not be sequential to the previous address. That is, the system begins fetching from the target address of the branch instruction. However, since the prediction won't be validated or

invalidated until the branch is finally executed, the fetching from the target is merely speculative, as opposed to known. Finally, it should be realized that the prediction (sequence signal) and the predicted address are determined/provided in the same cycle. This ensures that the pipeline will stay full by allowing a fetch to occur in the cycle just after the previous address. Say, for instance, that in cycle 0, a previous instruction is fetched from a previous address. In that same cycle, a signal specifying whether the branch is predicted taken/not taken will be appropriately set, and the current address will be determined based on that signal. Then in cycle 1, that current address may be fetched in cycle 1 (the very next cycle). As a result, pipeline disruption does not occur. If the signal and current address were not provided in the same cycle, then pipeline disruption would occur and the advantages gained through branch prediction would be at least partially nullified. This concept is further supported by pages 271-273 of Hennessy. That is, if a hit occurs in a branch buffer, then a prediction and a current address (in this case, the predicted address) are provided at the same time. See Fig.4.22 (note that the prediction and address are read from the buffer at the same time in response to a hit of the previous address).

6. Referring to claim 11, Yoshida has taught a system as described in claim 10. Yoshida has further taught an address control unit for receiving a branch condition, a branch decode signal, and a load/store signal, and for providing the first sequence signal. Clearly, it is inherent that each of these signals is present. A branch condition must be realized in order to determine the direction of the branch. In addition, since all instructions are decoded, including branches, a branch decode signal will be provided. And, load/store signals are inherent in any system with registers, which are clearly references in Fig.8-10 (Rn). Any components which receive these

signals are part of the address control unit. And, the first sequence signal is also provided by the address control unit.

7. Referring to claim 12, Yoshida has taught a system as described in claim 11. Yoshida has further taught:

a) an execution unit which provides the branch condition. See Fig.7, component 268, and note the condition code. Clearly, if the branch has to reference some condition in order to branch, then that condition must be produced by an execution unit. Usually, the condition is determined through operations such as addition.

b) a decode control unit which provides the branch decode signal and the load/store signal. See Fig.22, component 52, and note that since all instructions are decoded, signals corresponding to the instructions are produced by the decode unit.

8. Referring to claim 18, Yoshida has taught a processing system for fetching instructions and data, comprising:

a) an execution unit. See Fig.22, component 56.

b) a decode control unit. See Fig.22, component 52.

c) a fetch unit, coupled to the execution unit and the decode control unit, for providing data addresses on an address bus and for providing instruction addresses on the address bus to an instruction memory (Fig.25, component 11), the instruction memory having instructions stored at the instruction addresses, the fetch unit providing a first sequence signal that indicates whether each instruction address provided on the address bus is sequential to an immediately preceding instruction address even if a data address is provided between the instruction address and the immediately preceding instruction address, wherein, for each instruction address provided on the

address bus, the first sequence signal indicating whether the instruction address is sequential to an immediately preceding instruction address is provided with the instruction address for use by the instruction memory. Clearly, since Yoshida's system executes branches (see Fig.7), it must be determined if every instruction address is sequential to its preceding address. That is, every address will either be sequential to its preceding address or it will not be sequential due to a branch. Therefore, the first signal is merely any signal which dictates that a prediction is or is not to be used (and note from column 10, lines 30-36, that prediction is employed). For instance, a first signal exists which would cause the system to either use a predicted address for a branch (which could be non-sequential) or to use an incremented value of the program counter, a component that inherently exists. Based on the signal, an instruction address is generated for use by the instruction memory. Furthermore, it can be seen from Fig.27 that data addresses may occur between instruction addresses. It should be noted that even if a data address occurs between two instruction addresses, the system must still know whether the current instruction address is sequential or not sequential (whether to choose the next or a possible non-sequential prediction) to the previous instruction address, thereby requiring the existence of the first signal. Finally, it should be realized that the signal and the instruction address are determined in the same cycle (provided together). This ensures that the pipeline will stay full by allowing a fetch to occur in the cycle just after the previous address. For instance, say that in cycle 0, a previous instruction is fetched from a previous address. In that same cycle, a signal (for example, a BHT hit/miss signal) specifying whether a prediction is to be used or not will be appropriately set, and the current address will be determined based on that signal. Then in cycle 1, that current address may be fetch from in cycle 1 (the very next cycle). This ensures that no pipeline disruption

occurs. If the signal and current address were not provided in the same cycle, then pipeline disruption would occur and the advantages gained through branch prediction would be at least partially nullified. This is further supported by pages 271-273 of Hennessy. That is, if a hit occurs in a branch buffer, then a prediction and a current address (in this case, the predicted address) are provided at the same time. See Fig.4.22 (note that the prediction and address are read from the buffer at the same time in response to a hit of the previous address).

9. Referring to claim 19, Yoshida has taught a unit as described in claim 18. Yoshida has further taught that the execution unit comprises a condition generator that provides a branch condition signal to the fetch unit. See Fig.7, component 268, and note the condition code. Clearly, if the branch has to reference some condition in order to branch, then that condition must be produced by an execution unit. Usually, the condition is determined through operations such as addition.

10. Referring to claim 20, Yoshida has taught a unit as described in claim 19. Yoshida has further taught that the decode control unit provides a branch decode signal and a load/store signal to the fetch unit. See Fig.22, component 52, and note that since all instructions are decoded, signals corresponding to the instructions are produced by the decode unit.

Allowable Subject Matter

11. Claims 1-9, 13, 15-17, 21, 23-26 are allowed.

12. Claim 27 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

13. Applicant's arguments filed on January 30, 2006, have been fully considered but they are not persuasive.

14. Applicant argues the novelty/rejection of claim 10 on page 13 of the remarks, in substance that:

> "...unlike the branch target buffer of Hennessy, the instruction memory of claim 10 returns the instructions stored at the instruction addresses provided on the address bus. However, the branch target buffer of Hennessy checks the PC of an instruction to be fetched and if there is a hit, outputs another address (predicted PC for the target). That is, instructions are not provided from the branch target buffer of Hennessy."
>
> "...furthermore, there is no teaching to provide any branch prediction signal out with the next fetch address for use by an instruction memory. That is, once a prediction is made, this signal is no longer needed for that address, and it would unnecessarily complicate the system of Yoshida to provide this irrelevant and no longer needed signal along with the next fetch address."

15. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, the examiner agrees that the branch target buffer does not output instructions. However, the examiner is not relying on the branch target buffer (BTB) to be the claimed instruction memory. The instruction memory of Yoshida would simply be a cache, as shown in Fig.26, as is known in the art. The BTB outputs an address which is used by the memory to retrieve the instruction down the predicted branch path.

b) Applicant's claims do not require that the sequence signal be used by the instruction memory. There is no language in the claims which says "both the sequence signal and the current address are used by the instruction memory." Currently, only the "current address needs to be used by the instruction memory. In addition, even if it were made clear that current address and sequence signal are for use by the instruction memory, it is not clear how they are used by the memory in a way different from the prior art. For instance, in Yoshida, the examiner does not believe it

would be incorrect to say that Yoshida's main memory outputs an instruction based on a current address and a sequence signal. More specifically, the current address is obtained based on the value of the selection signal (i.e., its presence is necessary). So, in order for the instruction memory to output an instruction, it must use the sequence signal and the current address obtained from that signal's setting. Applicant should clarify how the instruction memory uses the signal and address.

16. The claim 18 arguments on page 14 of the remarks are similar to those for claim 10. Consequently, the examiner's response above also applies to the claim 18 arguments.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
March 31, 2006